a) ① Chapter 5.8

Word address	Binary address	Hit/Miss
1	1	Miss
134	10000110	Miss
212	11010100	Miss
1	1	Hit
135	10000111	Hit
213	11010101	Hit
162	10100010	Miss
161	10100001	Miss
2	10	Miss
44	101100	Miss
41	101001	Miss
221	11011101	Miss

Tag: Binary address >> 3 bits

Index (Binary address >> 1 bit) mod 4

Final contents (block addresses): Set 00: 0, 10100000, 10100

Set 01: 10100010, 10

Set 10: 11010100, 10110

Set 11: 10000110

1 01 → 58

(b)

Word address	Binary address	Hit/Miss
6	110	Miss
124	1111100	Miss
175	10101111	Miss
214	11010110	Hit
6	110	Hit
84	1010100	Miss
65	1000001	Miss
174	10101110	Hit
64	1000000	Miss
105	1101001	Miss
85	1000	Hit
215	11010111	Hit

Tag = Binary address >> 3 bits

Index (or set #): (Binary address >> 1 bit) mod 4

Final cache contents

set: blocks (3 slots for 2-word blocks per set)

00 : 01000000, 01000000, 01101000

01 :

10 : 01010100

11 : 0000010, 1101011 0, 10101110

2 of chapter 5-8

Word address	Binary address	Hit/Miss
1	1	Miss
134	10000110	Miss
212	11010100	Miss
1	1	Hit
135	10000111	Miss
213	11010101	Miss
162	10100010	Miss
161	10100001	Miss
2	10	Miss
44	101100	Miss
41	101001	Miss
221	11011101	Miss

Tag: Binary address

Index: None (only one set)

Hit/Miss: M, M, M, H, M, M, M, M, M, M, M, M

Final contents (block addresses)

10000111, 11010101, 10100001, 10, 101100, 101001,

— 11011101

(b)

Word ad	Binary address	Hit/Miss
6	110	Miss
124	1111100	Miss
175	10101111	Miss
214	11010110	Hit
6	110	Hit
84	1010100	Miss
65	1000001	Miss
174	10101110	Miss
64	1000000	Miss
105	1101001	Miss
85	1000	Miss
215	11010111	Miss

Binary address: (bits 7-0 tag, no index or block offset

Tag: Binary address

Final cache contents (block address) (8 cache slots 1-word per cache slot)

a) 00000110 | c) 01010101 | f) 10101110 | i) 01010101

b) 11010110 | d) 11010111 | g) 01000000 | 11010111

e) 01000001 | i) 01101001

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(a)

Word address	Binary address
1	1
134	10000110
212	11010100
1	1
135	10000111
213	11010101
162	10100010
161	10100001
2	10
44	101100
41	101001
221	11011101

Hit/Miss:
LRU: M, M, M, H, H, H, M, M, M, M, M, M

Hit/Miss
MRU
M, M, M, H, H, H, M, M, M, M, M, M.

Given 2 word blocks the best miss rate is 9/12

(b) Binary address: (bits 7-1 tag, 1 block offset
8 cache slots, 2 words per cache slot

Word address	Binary	Hit/Miss
6	110	Miss
124	1111100	Miss
175	10101111	Miss
214	11010110	Hit
6	110	Hit
84	1010100	Miss
65	10000001	Miss
174	10101110	Hit
64	1000000	Hit
105	1101001	Miss
85	1000	Hit
215	11010111	Hit

No need for LRU or MRU replacement policy, hence best missRate is 6/12

④ → chapt 5.8

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② base CPI = 2.0

Memory miss cycles: 125 cycles / (1/3) ns/clock = 375 clock cycles

1. Total CPI = base CPI + memory miss cycles × 1st level cache miss rate
2. Total CPI = base CPI + memory miss cycles × global miss rate w/ 2nd level direct mapped cache + 2nd level direct-mapped speed × 1st level cache miss rate
3. Total CPI = base CPI + memory miss cycle × global miss rate w/ 2nd level 8-way set assoc. cache + 2nd level 8-way set assoc. speed × 1st level cache miss rate

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ⓑ

1. Total CPI : 2,0 + 375 × 5% = 20.75 / 39,5 / 11,375 (normal/double/h
2. Total CPI = 2,0 + 15 × 5% + 375 × 3% = 14 / 25,25 / 8,375
3. Total CPI : 2,0 + 25 × 5% + 375 × 1,8% = 10 / 16,75 / 6,625

ⓒ Base CPI: 2,0

Memory miss cycles: 100 clock cycles

1. Total CPI = base CPI + memory miss cycles × 1st level cache miss rate
2. Total CPI = base CPI + memory miss cycles × global miss rate w/ 2nd level direct mapped cache + 2nd level direct-mapped speed × 1st level cache miss rate
3. Total CPI = base CPI + memory miss cycles × global miss rate w/ 2nd level 8-way set assoc cache + 2nd level 8-way set assoc speed × 1st level cache miss rate

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ⓓ

1. Total CPI (using 1st level cache): 2,0 + 100 × 0,04 = 6
2. Total CPI (using 1st level cache): 2,0 + 200 × 0,04 = 10
3. Total CPI (" " " ") : 2,0 + 50 × 0,04 = 4,0

ⓔ

4e of chapter 5.8

a. Total CPI (using 2nd level direct-mapped cache: =
= 2,0 + 100 x 0,04 + 10 x 0,04 = 6.4

2. Total CPI (using 2nd level direct-mapped cache) =
= 2,0 + 200 x 0,04 + 10 x 0,04 = 82.4

a Total CPI (using 2nd level direct-mapped cache) =
= 2,0 + 50 x 0,04 + 10 x 0,04 = 4.4

(g) Total CPI (using 2nd level 8-way set assoc. cache) =
= 2,0 + 100 x 0,016 + 20 x 0,04 = 44

Total CPI (using 2nd level 8-way set assoc. cache) =
= 2,0 + 200 * 0,016 + 20 x 0,04 = 6

Total CPI (using 2nd level 8-way set assoc cache:) =
= 2.0 + 50 x 0,016 + 20 x 0,04 = 3.6

(5) → chap 5.8

(a) Let us consider base CPI = 2

Memory miss cycles = $\frac{125 \text{ cycles}}{\frac{1}{3} \text{ ns/clock}}$

= 375 clock cycles

Total CPI = base CPI + memory miss cycles * global miss rate + second level direct mapped cache + second level direct mapped speed * first level cache miss rate

step 2

Therefore the total CPI = 2 + 15 × 5% + 50 × 3% + 375 × 1.3%

= 2 + 0,75 + 1.5 + 4.875

= 9.125

∴ CPI = 9.125

step 3

This provides better performance and this is more complex cache coherency, increased cycle time and larger and more expensive chips

step 4

(b) Let us consider base CPI = 2

Memory miss cycles = 100 clock cycles

Total CPI = baseCPI + memory miss cycles * global miss rate + second level direct mapped cache + second level direct mapped speed * first level cache miss rate.

Therefore the total CPI = 2 + 100 × 0,04 + 10 × 0,04 =

= 6.4

step 5

Total CPI = base CPI + memory miss cycles * global miss rate + third level direct mapped cache + second level direct mapped speed * first level cache miss rate + third level direct mapped speed * 2nd level cache miss rate.

Therefore the total CPI = 2 + 100 × 0,013 + 10 × 0,04 + 50 × 0,04

< 2 + 1.3 + 0,4 + 2 = 5.7

5 → chap 5.8

step 6

TOTAL CPI

$\therefore CPI = 5.7$

This provides better performance and this is more complex cache coherency, increased cycle time and larger and more expensive chips

6 from chap 5.8

a.) Let us consider base CPI = 2

Memory miss cycles = $\frac{125 \text{ cycles}}{\frac{1}{3} \text{ ns/clock}}$

= 375 clock cycles

Total CPI = base CPI + cache access time × first level cache miss rate + memory miss cycles ~~× global miss rate 0,7%~~ × (global miss rate 0,7% × n)

Therefore the total CPI = 2 + 50 × 5% + 375 × (4% − 0,7% × n)

= CPI = 1.4

Now n = 3 then 2MB L2 cache to match DM

And n = 4 then 2.5 MB L2 cache to match 2-way

b) Let us consider CPI = 2.

Memory miss cycles = 100 clock cycles

Total CPI (using 2nd level direct-mapped cache) = 2 + 100 × 0,04 + 10 × 0,0

= 6.4

total CPI (using 2nd level 8-way set assoc cache = 2 + 100 × 0,016 + 20 × 0,04 =

= 4.4

total CPI = base CPI + cache access time × first level cache miss rate + memory miss cycles × (global miss rate − 0,7% × n)

Therefore the total CPI = 2 + 50 × 0,04 + 100 × (0,04 − 0,007 × n

Here n = 0 then total CPI = 8

n = 1 " " " = 7.3

n = 2 ⟶ CPI = 6.6

n = 3 ⟶ CPI = 5.9

n = 4 ⟶ CPI = 5.7

n = 5 ⟶ CPI is 5

the match 2nd level direct mapped cache CPI, n = 4 or 4 MB L2 cache, and to match 2nd level 8-way set assoc cache CPI, n = 5 MB or 3 MB L2 cache